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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,440	01/20/2004	George E. Hanson	03-1597	9224

24319 7590 03/10/2006

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EXAMINER	
BERHANE, ADOLF D	

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/760,440	HANSON, GEORGE E.	
	Examiner	Art Unit	
	Adolf Berhane	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-14 and 16-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-14 and 16-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6, 8-14 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushita (6,504,270).

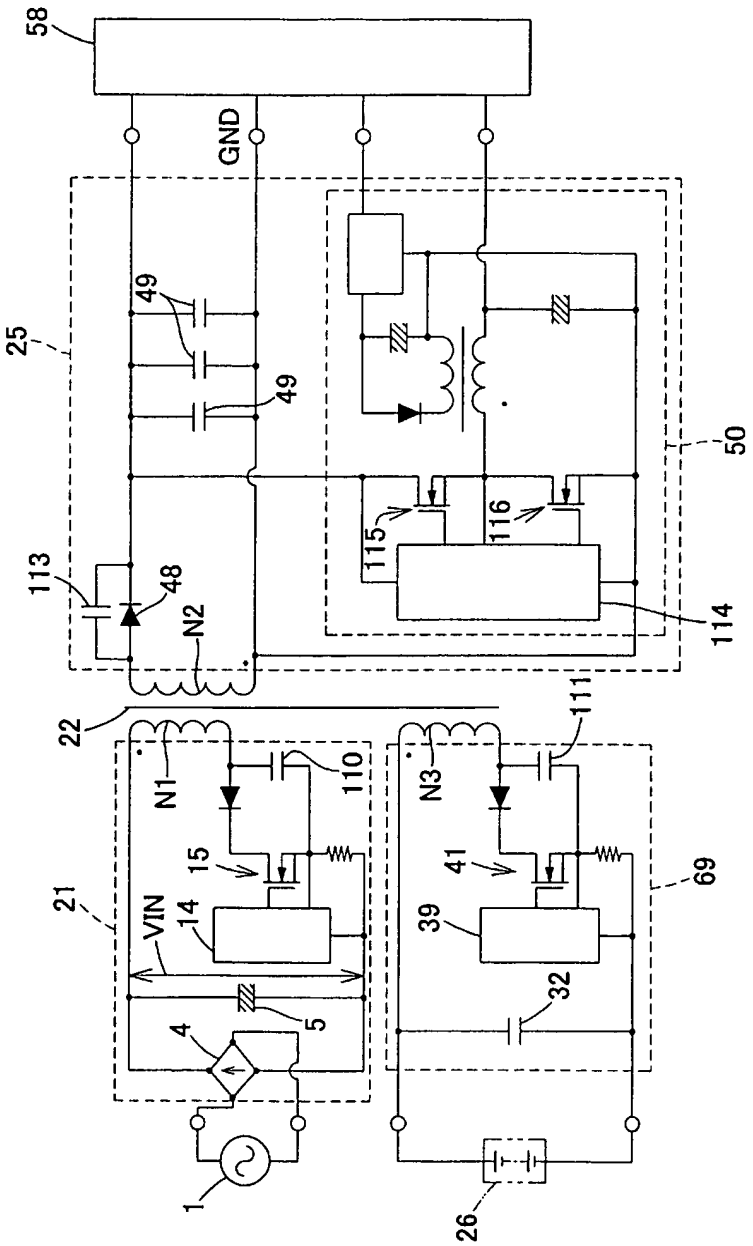
Matsushita teach the claimed invention except for a full wave rectifier at the output of the transformer. Matsushita disclose an uninterruptible switching regulator in Figs. 1-7. A DC output stage that outputs a predetermined DC electrical power (+12), an AC input stage (1) connected to the DC output stage (+12 V, -12 V and +5 V, see Fig. 4), with the AC input stage (1) configured to convert AC electrical power at the AC input stage into the predetermined DC electrical power (4) available at the DC output stage, a DC input stage (26) connected to the DC output stage, with the DC input stage configured to convert DC electrical power at the DC input stage into the predetermined DC electrical power (50) available at the DC output stage, the DC output stage comprises at least one capacitor (49) across a DC positive output terminal and a DC ground output terminal (+12 V, -12 V and +5 V, see Fig. 4), an AC sense circuit (8) that detects AC electrical power at the AC input stage, the DC input stage (30) comprises a DC input stage disable line connected to the AC sense circuit, and wherein the DC input stage disable line (34) disables outputting the predetermined DC electrical power from

the DC input stage when the AC sense circuit detects AC electrical power at the AC input stage, a switching circuit (69) that receives the DC electrical power and that is configured to generate a substantially AC waveform at a first AC voltage level from the DC electrical power, a transformer (22) connected to the switching circuit and configured to convert the substantially AC waveform at the first AC voltage level to a second AC voltage level; and a rectifier (48) connected to the transformer and configured to convert the substantially AC waveform at the second AC voltage level to the predetermined DC electrical power, a buffer stage (15 & 41) connected to the switching circuit and configured to provide electrical current to the substantially AC waveform. Matsushita teach the use of a full wave rectifier in Fig. 4 (3 and 4). It would have been obvious to one having ordinary skill in the art at the time of the invention to replace the rectifier (48) with a full wave rectifier as taught in Fig. 4, in order to provide full wave rectification with one element functions during positive half-cycles and the other during negative half-cycles.

Response to Arguments

3. Applicant's arguments filed 1/19/06 have been fully considered but they are not persuasive.

Fig. 1


58
GND
49
49
25
50
116
115
113
48
N2
114
22
111
N1
110
N3
15
41
69
21
VIN
14
39
32
5
4
1
26

Applicant's attention is directed to Fig. 1 which examiner would not only identify the elements with the claimed language but also with Applicant's Fig. 3. Applicant's Fig. 3 elements are identified with Matsushita element. Applicant's element 102 (Matsushita's 21), DC input (26), filter 140 (32), driver circuit 341 (39), switches 34 (41), transformer 343 (22), rectifier 142 (48) and capacitor C1 (49). With respect to Fig. 1 of Matsushita patent, a DC output stage that outputs a predetermined DC electrical power (25), an AC input stage (21) connected to the DC output stage (25), with the AC input stage (21) configured to convert AC electrical power at the AC input stage into the predetermined DC electrical power (21) available at the DC output stage, a DC input stage (26) connected to the DC output stage, with the DC input stage configured to convert DC electrical power at the DC input stage into the predetermined DC electrical power (50) available at the DC output stage, the DC output stage comprises at least one capacitor (49) across a DC positive output terminal and a DC ground output terminal (25), an AC sense circuit (8) that detects AC electrical power at the AC input stage, the DC input stage (30) comprises a DC input stage disable line connected to the AC sense circuit, and wherein the DC input stage disable line (34) disables outputting the predetermined DC electrical power from the DC input stage when the AC sense circuit detects AC electrical power at the AC input stage, a switching circuit (69) that receives the DC electrical power and that is configured to generate a substantially AC waveform at a first AC voltage level from the DC electrical power, a transformer (22) connected to the switching circuit and configured to convert the substantially AC waveform at the first AC voltage level to a second AC voltage level; and a rectifier (48) connected to the

transformer and configured to convert the substantially AC waveform at the second AC voltage level to the predetermined DC electrical power, a buffer stage (15 & 41) connected to the switching circuit and configured to provide electrical current to the substantially AC waveform. Matsushita teach the use of a full wave rectifier in Fig. 4 (3 and 4). It would have been obvious to one having ordinary skill in the art at the time of the invention to replace the rectifier (48) with a full wave rectifier as taught in Fig. 4, in order to provide full wave rectification with one element functions during positive half-cycles and the other during negative half-cycles.

In re McLaughlin, 170 USPQ 209 (CCPA 1971)

The test for combining references is not what the individual references themselves suggest but rather what the combination of the disclosures taken as a whole would suggest to one of ordinary skill in the art.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adolf Berhane whose telephone number is 571-272-2077. The examiner can normally be reached on Monday- Friday 8 AM to 6 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Karl Easthom can be reached on 571-272-1989. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Adolf Berhane
Primary Examiner
Art Unit 2838